AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) A method of transmitting signals in a network comprising:
receiving a first signal and a second adjacent signal;
sensing simultaneous ~~transition~~ transitions of the first signal and the second signal;
delaying the first signal for a time period based on the simultaneous transitions of the first signal and the second signal;
switching the second signal; and
switching the first signal after the time period.

2. (Original) The method of claim 1 wherein
sensing is performed by a sensing and delay circuit.

3. (Original) The method of claim 1 wherein
the first signal is delayed by a first buffer before switching; and
the second signal is delayed by a second buffer before switching.

4. (Original) The method of claim 3 wherein
sensing is performed by a sensing and delay circuit.

5. (Original) The method of claim 4 wherein
the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until after the second signal switches.

6. (Currently amended) The method of claim 1 further comprising:
receiving a third signal wherein the first signal is adjacent to the second and the third signal;
sensing simultaneous ~~transition~~ transitions of the third signal ~~with~~ and the first signal;
delaying the first signal for a time period based on the simultaneous transitions of the third signal and the first signal;

switching the third signal; and
switching the first signal after the time period.

7. (Original) The method of claim 6 wherein
sensing is performed by a sensing and delay circuit.

8. (Original) The method of claim 7 wherein
the first signal is delayed by a first buffer before switching;
the second signal is delayed by a second buffer before switching, and
the third signal is delayed by a third buffer before switching.

9. (Original) The method of claim 8 wherein
sensing is performed by a sensing and delay circuit.

10. (Original) The method of claim 9 wherein
the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until after the second signal and third signal switches.

11. (Original) A method of transmitting signals in a network comprising:
receiving a first, a second, a third, a fourth, and a fifth adjacent signals;
sensing transitions of the first, the second, the third, the fourth, and the fifth signals;
delaying switching of the first signal in the event the second signal transitions at the same time as the first signal;
delaying switching of the third signal in the event the second and fourth signals transition at the same time as the third signal; and
delaying switching of the fifth signal in the event the fourth signal transitions at the same time as the fifth signal.

12. (Original) The method of claim 11 wherein
sensing is performed by a sensing and delay circuit.

13. (Original) The method of claim 11 wherein
the first signal is delayed by a first buffer before switching;
the second signal is delayed by a second buffer before switching;
the third signal is delayed by a third buffer before switching;
the fourth signal is delayed by a fourth buffer before switching; and
the fifth signal is delayed by a fifth buffer before switching.

14. (Original) The method of claim 13 wherein
sensing is performed by a sensing and delay circuit.

15. (Original) The method of claim 14 wherein
the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until the second signal switches;
the sensing and delay circuit provides a delay signal to the third buffer and delays the third signal until the second and the fourth signal switch; and
the sensing and delay circuit provides a delay signal to the fifth buffer and delays the fifth signal until the fourth signal switches.

16. (Currently amended) A signal transmitting network comprised of
a device configured to:
receive a first signal and a second adjacent signal;
sense simultaneous ~~transition~~ transitions of the first signal and the second signal;
delay the first signal for a time period based on the simultaneous transitions of the first signal and the second signal;
switch the second signal; and
switch the first signal after the time period.

17. (Currently amended) A signal transmitting network comprised of:
a first device configured to:
receive a first signal and a second adjacent signal;
delay the first signal for a time period;
switch the second signal; and

switch the first signal after the time period; and

a second device configured to:

sense simultaneous ~~transition~~ transitions of the first signal and the second signal, wherein the first signal is delayed based on the simultaneous transitions of the first signal and the second signal.

18. (Original) The signal transmitting network of claim 16 further comprised of:

a first buffer that delays the first signal before switching; and

a second buffer that delays the second signal before switching.

19. (Original) The signal transmitting network of claim 18 wherein

sensing is performed by a sensing and delay circuit.

20. (Original) The signal transmitting network of claim 19 wherein

the second device provides a delay signal to the first buffer and delays the first signal until after the second signal switches.

21. (Currently amended) The signal transmitting network of claim 16 wherein the device is further configured to:

receive a third signal wherein the first signal is adjacent to the second and third signal;

sense simultaneous ~~transition~~ transitions of the third signal ~~with~~ and the first signal;

delay the first signal for a time period based on the simultaneous transitions of the third signal and the first signal;

switch the third signal; and

switch the first signal after the time period.

22. (Currently amended) A signal transmitting network comprised of:

a first device configured to:

receive a first signal, a second signal, and third signal wherein the first signal is adjacent to the second signal and the third signal;

delay the first signal for a time period; and

switch the third signal, and the first signal after the time period; and

a second device configured to:

sense simultaneous transitions of the first signal and the third signal,

wherein the first signal is delayed based on the simultaneous transitions of the first signal and the third signal.

23. (Original) The signal transmitting network of claim 22 wherein
the first signal is delayed by a first buffer before switching;
the second signal is delayed by a second buffer before switching, and
the third signal is delayed by a third buffer before switching.

24. (Original) The signal transmitting network of claim 23 wherein the second device is a sensing and delay circuit.

25. (Currently amended) The signal transmitting network of claim 24 wherein the second device provides a delay signal to the first buffer and delays the first signal until after the second signal and the third signal ~~switches~~ switch.

26. (Original) A signal transmitting network comprised of
a device configured to:

receive a first, a second, a third, a fourth, and a fifth adjacent signals;

sense transitions of the first, the second, the third, the fourth, and the fifth signals;

delay switching of the first signal in the event the second signal transitions at the same time as the first signal;

delay switching of the third signal in the event the second and fourth signals transition at the same time as the third signal; and

delay switching of the fifth signal in the event the fourth signal transitions at the same time as the fifth signal.

27. (Original) A signal transmitting network comprised of:
a first device configured to:

receive a first, a second, a third, a fourth, and a fifth adjacent signals;

delay switching of the first signal in the event the second signal transitions at the same time as the first signal;

delay switching of the third signal in the event the second and fourth signals transition at the same time as the third signal; and

delay switching of the fifth signal in the event the fourth signal transitions at the same time as the fifth signal; and

a second device configured to:

sense transitions of the first, the second, the third, the fourth, and the fifth signals.

28. (Original) The signal transmitting network of claim 26 wherein

the first signal is delayed by a first buffer before switching;

the second signal is delayed by a second buffer before switching;

the third signal is delayed by a third buffer before switching;

the fourth signal is delayed by a fourth buffer before switching; and

the fifth signal is delayed by a fifth buffer before switching.

29. (Original) The signal transmitting network of claim 28 wherein

sensing is performed by a sensing and delay circuit.

30. (Original) The signal transmitting network of claim 29 wherein

the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until the second signal switches;

the sensing and delay circuit provides a delay signal to the third buffer and delays the third signal until the second and the fourth signal switch; and

the sensing and delay circuit provides a delay signal to the fifth buffer and delays the fifth signal until the fourth signal switches.

31. (Currently amended) An apparatus for transmitting signals in a network comprised of:

means for receiving a first signal and a second adjacent signal;

means for sensing simultaneous ~~transition~~ transitions of the first signal and the second signal;

means for delaying the first signal for a time period based on the simultaneous transitions of the first signal and the second signal;

means for switching the second signal; and

means for switching the first signal after the time period.

32. (Original) The apparatus claim 31 wherein

the means for sensing is performed by a sensing and delay circuit.

33. (Original) The apparatus of claim 31 wherein

the first signal is delayed by a first buffer before switching; and

the second signal is delayed by a second buffer before switching.

34. (Original) The apparatus of claim 33 wherein

the means for sensing is performed by a sensing and delay circuit.

35. (Original) The apparatus of claim 34 wherein

the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until after the second signal switches.

36. (Currently amended) The apparatus of claim 31 further comprising:

means for receiving a third signal wherein the first signal is adjacent to the second and the third signal;

means for sensing simultaneous transition of the third signal ~~with~~ and the first signal;

means for delaying the first signal for a time period based on the simultaneous transitions of the third signal and the first signal;

means for switching the third signal; and

means for switching the first signal after the time period.

37. (Original) The apparatus of claim 36 wherein

the means for sensing is performed by a sensing and delay circuit.

38. (Original) The apparatus of claim 37 wherein
the first signal is delayed by a first buffer before switching;
the second signal is delayed by a second buffer before switching, and
the third signal is delayed by a third buffer before switching.

39. (Original) The apparatus of claim 38 wherein
the means for sensing is performed by a sensing and delay circuit.

40. (Original) The apparatus of claim 39 wherein
the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until after the second signal and third signal switches.

41. (Currently amended) An apparatus [[of]] for transmitting signals in a network comprising:
means for receiving a first, a second, a third, a fourth, and a fifth adjacent signals;
means for sensing transitions of the first, the second, the third, the fourth, and the fifth signals;
means for delaying switching of the first signal in the event the second signal transitions at the same time as the first signal;
means for delaying switching of the third signal in the event the second and fourth signals transition at the same time as the third signal; and
means for delaying switching of the fifth signal in the event the fourth signal transitions at the same time as the fifth signal.

42. (Original) The apparatus of claim 41 wherein
the means for sensing is performed by a sensing and delay circuit.

43. (Original) The apparatus of claim 41 wherein
the first signal is delayed by a first buffer before switching;
the second signal is delayed by a second buffer before switching;
the third signal is delayed by a third buffer before switching;
the fourth signal is delayed by a fourth buffer before switching; and

the fifth signal is delayed by a fifth buffer before switching.

44. (Currently amended) The apparatus of claim 43 wherein
the means for sensing is ~~performed by~~ a sensing and delay circuit.

45. (Original) The apparatus of claim 44 wherein
the sensing and delay circuit provides a delay signal to the first buffer and delays the first signal until the second signal switches;
the sensing and delay circuit provides a delay signal to the third buffer and delays the third signal until the second and the fourth signal switch; and the sensing and delay circuit provides a delay signal to the fifth buffer and delays the fifth signal until the fourth signal switched.

46. (Previously Presented) An apparatus comprising:
a circuit configured to detect a transition of a first signal and a transition of a second signal and provide a delay signal when the transitions of the first and the second signals occur simultaneously; and
a first buffer coupled to the circuit, wherein the first buffer is configured to delay the transition of the first signal in response to the delay signal.

47. (Previously Presented) The apparatus of claim 46, wherein the first buffer is configured to delay the transition of the first signal until the transition of the second signal has completed.

48. (Previously Presented) The apparatus of claim 46, wherein
the circuit is further configured to detect a transition of a third signal and provide the delay signal when the transitions of the first and third signals occur simultaneously.

49. (Previously Presented) The apparatus of claim 48, wherein the first buffer is further configured to delay the transition of the first signal until the transition of the third signal has completed.

50. (Previously Presented) The apparatus of claim 48 further comprising:

a second buffer configured to receive the second signal and provide a delayed second signal, wherein a delay of the second buffer is equal to an inherent delay of the first buffer; and

a third buffer configured to receive the third signal and provide a delayed third signal, wherein a delay of the third buffer is equal to the inherent delay of the first buffer.

51. (Previously Presented) The apparatus of claim 50 wherein the first signal is adjacent to the second signal and the third signal.

52. (Previously Presented) The apparatus of claim 50 further comprising:

a first sense signal, wherein the first signal is coupled to the circuit via the first sense signal;

a second sense signal, wherein the second signal is coupled to the circuit via the second sense signal; and

a third sense signal,wherein the third signal is coupled to the circuit via the third sense signal.

53. (Previously Presented) The apparatus of claim 46 further comprising:

an integrated circuit coupled to the circuit.

54. (Previously Presented) An apparatus comprising:

a circuit configured to detect a transition of each signal of a plurality of signals and provide a delay signal when any adjacent signals simultaneously transition; and

a plurality of buffers coupled to the circuit, wherein at least one buffer of the plurality is configured to delay at least one transition in response to the delay signal.

55. (Previously Presented) The apparatus of claim 54, wherein the at least one buffer is configured to delay the at least one transition until all adjacent transitions to the at least one transition have completed.

56. (Previously Presented) The apparatus of claim 54, further comprising:

a first circuit configured to detect a transition of a first signal and a transition of a second signal and provide a first delay signal when the transitions of the first and second signals occur simultaneously; and

a first buffer coupled to the first circuit, wherein the first buffer is configured to delay the transition of the first signal in response to the first delay signal.

57. (Previously Presented) The apparatus of claim 56, wherein the first signal is adjacent to the second signal.

58. (Previously Presented) The apparatus of claim 57, wherein in response to the first delay signal the first buffer is further configured to delay the transition of the first signal until the transition of the second signal has completed.

59. (Previously Presented) The apparatus of claim 56, further comprising:

a second circuit configured to detect a transition of the second signal, a transition of a third signal, and a transition of a fourth signal and provide a second delay signal when the transition of the third signal occurs simultaneously with at least one of the transition of the second signal and the transition of the fourth signal; and

a second buffer coupled to the second circuit, wherein the second buffer is configured to delay the transition of the third signal in response to the second delay signal.

60. (Previously Presented) The apparatus of claim 59, wherein the third signal is adjacent to the second signal and the fourth signal.

61. (Previously Presented) The apparatus of claim 59, wherein in response to the second delay signal the second buffer is further configured to delay the transition of the third signal until the transition of at least one of the third signal and the fourth signal has completed.

62. (Previously Presented) The apparatus of claim 59, further comprising:

a third circuit configured to detect a transition of the fourth signal and a transition of a fifth signal and provide a third delay signal when the transitions of the fourth and fifth signals occur simultaneously; and

a third buffer coupled to the third circuit, wherein the third buffer is configured to delay the transition of the fifth signal in response to the third delay signal.

63. (Previously Presented) The apparatus of claim 62, wherein the fourth signal is adjacent to the fifth signal.

64. (Previously Presented) The apparatus of claim 62, wherein in response to the third delay signal the third buffer is further configured to delay the transition of the fifth signal until the transition of the fourth signal has completed.

65. (Previously Presented) The apparatus of claim 62 further comprising:

a fourth buffer configured to receive the second signal and provide a delayed second signal, wherein a delay of the second buffer is equal to an inherent delay of the first buffer; and

a fifth buffer configured to receive the fourth signal and provide a delayed fourth signal, wherein a delay of the fifth buffer is equal to the inherent delay of the third buffer.

66. (Previously Presented) The apparatus of claim 54, further comprising:

a second circuit configured to detect a transition of each signal of a second plurality of signals and provide a second delay signal when any adjacent signals simultaneously transition;

a second plurality of buffers coupled to the second circuit, wherein at least one buffer of the second plurality is configured to delay at least one transition in response to the second delay signal; and

a shield line between the plurality of signals and the second plurality of signals.